THE PATENT S ACT, 1970 **Date: 23/05/2019**

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THE PATENTS RULES, 2003

SECTION 15

In the matter of Application number : 3304/DEL/2005

DECISION

Applicant - MICROSOFT TECHNOLOGY LICENSING, LLC.

Attorney Present for hearing : Ankur Garg from Lakshmi Kumaran & Sridharan.

An application number **3304/DEL/2005** entitled "REVERSIBLE 2-DIMENSIONAL PRE-/POST-FILTERING FOR LAPPED BIORTHOGONAL TRANSFORM " was filled at Patent Office, Mumbai on 08/12/2005 for grant of Patent.

The facts of the application are as fallow:

S.NO	Detail of the application	Dates of activity
1	Application No **3304/DEL/2005**	Filled on 08/12/2005
2		-
3	Request for examination filed	31/12/2008
4	Publication U/S 11(A)	02/10/2009
5	FER was issued to the Applicant	29/01/2015
6	Reply to First Examination Report	12/10/2015
7	Hearing notice	30/01/2019
8	Hearing date	01/03/2019
9	Written submission after hearing	15/03/2019

A hearing notice was sent to the applicant with the following outstanding objections:

Objections

1. The subject matter as described and claimed in claims lack inventive step in the view of following prior art documents: D2: WO0051014 (A2) - (MICROSOFT CORP [US]), 31st Aug, 2000: MODULATED COMPLEX LAPPED TRANSFORM FOR INTEGRATED SIGNAL ENHANCEMENT AND CODING D3: US5859788 (A) - (FUJITSU LTD [US]), 12th Jan, 1999: Modulated lapped transform method D4:

US6771828 (B1) - (MICROSOFT CORP [US]), 3rd Aug, 2004: System and method for progessively transform coding digital data D2 discloses system and method for performing spectral analysis (1500) of a digital signal having a discrete duration by spectrally decomposing the digital signal at predefined frequencies uniformly distributed over a sampling frequency interval into complex frequency coefficients (220, 222) so that magnitude and phase information at each frequency is immediately available to produce a modulated complex lapped transform (MCLT). The present invention includes a MCLT processor (1510), an acoustic echo cancellation device (1512) and a noise reducer (1514) integrated with an encoder/decoder device (1500). Further to the disclosure of D2, D3 discloses a forward transform method for forward transforming a plurality of windows of input data respectively into a plurality of blocks of forward transformed data by a forward transform defined by a window function and a modulation function, each window is segmented into a plurality of blocks of input data, each block of input data and each block of forward transformed data have a predetermined block size k, each window has a predetermined window size n and n/k is a positive integer greater than one, each window has an overlapping block of input data in common with another adjacent window of the plurality of windows, wherein the improvement comprises, multiplying forward window values by each window of input data for providing window product data for each window, filtering the window product data for providing a block of forward transformed data, and repeating the multiplying and filtering steps for each successive window of the plurality of windows of input data for providing the respective plurality of blocks of forward transformed data. D4 discloses a system and method for compressing image data using a lapped biorthogonal transform (LBT). The present invention encodes data by generating coefficients using a hierarchical LBT, reorders the coefficients in a data-independent manner into groups of similar data, and encodes the reordered coefficients using adaptive run-length encoding. The hierarchical LBT computes multi resolution representations. The use of the LBT allows the present invention to encode image data in a single pass at any desired compression ratio and to make use of existing discrete cosine transform (DCT) software and hardware modules for fast processing and easy implementation. Thus, when the concepts described in D2 and D3 is coupled with the teachings of D4; the subject matter of claims would be obvious to a person skilled in the art. Hence, as such claims does not constitute an invention u/s 2(1)(j) of The Patent Act, 1970.

2. Submission of the applicant has been considered. However, the alleged invention falls within the scope of section 3(k) of the Patents Act as: The applicant in its reply to FER dated 12.10.2015 states “The Applicant would like to submit that the invention as claimed in any claims is a novel computer program implemented on a known computer” in last paragraph on page 4. Guidelines for Examination of Computer-related Inventions (CRIs) published on 19.02.2016 and issued vide office order no. CG/office order/2016/179 dated 19.02.2016, in chapter 5 on page 18 states: “If the contribution lies in the field of computer programme, check whether it is claimed in conjunction with a novel hardware and proceed to other steps to determine patentability with respect to the invention. The computer programme in itself is never patentable. If the contribution lies solely in the computer programme, deny the claim. If the contribution lies in both the computer programme as well as hardware, proceed to other steps of patentability.” Hence, in the view of contribution lying solely in the computer programme, claims 1-15 are not allowable under section 3(k) of the Patents Act, 1970 (as amended).

Agent for the applicant had attended the hearing held on 01/03/2019 and the outstanding objections were discussed. The applicant submitted his written submission on 15/03/2019.

Agent for the applicant in their written submission argued in respect of Para 1 that :

Invention u/s 2(1)(j) Objection 1 -

The subject matter as described and claimed in claims lack inventive step in the view of following prior art documents: D2: WO0051014 (A2) - (MICROSOFT CORP [US]), 31st Aug, 2000: MODULATED COMPLEX LAPPED TRANSFORM FOR INTEGRATED SIGNAL ENHANCEMENT AND CODING D3: US5859788 (A) - (FUJITSU LTD [US]), 12th Jan, 1999: Modulated lapped transform method D4: US6771828 (B1) - (MICROSOFT CORP [US]), 3rd Aug, 2004. [[Remaining objection has not been reproduced for the sake of brevity]] 1.1 Through the present objection, the Learned Assistant Controller has objected that the subject matter of pending claim 1-15 is not inventive u/s 2(1)(ja) of the Indian patent act 1970 w.r.t. D2-D4, where D2: WO0051014 (A2), D3: US5859788 (A), and D4: US6771828 (B1) 1.2 The Applicant humbly submitted to the Learned Assistant Controller that the pending claims involve an inventive step when considered in view of the cited prior arts D2-D4. 1.3 The Applicant submits that D2 relates to a system and method for performing spectral analysis of a digital signal having a discrete duration. The spectral analysis is performed by spectrally decomposing the digital signal at predefined frequencies uniformly distributed over a sampling frequency interval into complex frequency coefficients so that magnitude and phase information at each frequency is immediately available to produce a modulated complex lapped transform (MCLT). In operation, the system produces a modulated complex lapped transform (MCLT) and includes real and imaginary window processors and real and imaginary transform processors. Each window processor has window functions and operators. The real window processor receives the input signal as sample blocks and applies and computes butterfly coefficients for the real part of the signal to produce resulting real vectors. The imaginary window processor receives the input signal as sample blocks and applies and computes butterfly coefficients for the imaginary part of the signal to produce resulting imaginary vectors. The real transform processor computes a spatial transform on the real vectors to produce a real transform coefficient for the MCLT. The imaginary transform processor computes a spatial transform on the imaginary vectors to produce an imaginary transform coefficient for the MCLT. In addition, the system can include inverse transform module for inverse transformation of the encoded output. The inverse transform module can include components that are the exact inverse of the inverse real and imaginary transform processors and the real and imaginary inverse window processors. The encoded output is received and processed by inverse real and imaginary transform processors, and then received and processed by real and imaginary inverse window processors to produce an output signal that substantially matches the input signal. 1.4 The Applicant further submits that D3 discloses techniques for fast modulated lapped transform (MLT). The MLT minimizes blocking artifacts associated with JPEG based discrete cosine transform (DCT) image compression systems. The MLT method combines fast block processing capabilities of wavelet transforms and fast block processing of DCT image compression systems. The modular and pipeline MLT architecture is fast by block processing but avoids the visual blocking artifacts that can be seen in most DCT-based compression systems. The improved MLT processors are implemented by an infinite impulse response filter operating on a product of the MLT window function and the input data stream. Forward and reverse MLT processors include a new fused multiply-add logic for fast computations and localized interconnections. The MLT processors can be combined into a bank of parallel processors in a one-dimensional MLT architecture, which can be used for two-dimensional image transformation. The improved MLT implementation enables a modular architecture having a reduced number of multipliers and interconnects well suited for practical VLSI implementation. 1.5 The Applicant submits that D4 further relates to techniques for compressing image data using a lapped biorthogonal transform (LBT). In operation, the techniques include encoding of data by generating coefficients using a hierarchical LBT, reordering the coefficients in a data-independent

manner into groups of similar data, and encoding the reordered coefficients using adaptive run-length encoding. The hierarchical LBT computes multiresolution representations. The use of the LBT allows to encode image data in a single pass at any desired compression ratio and to make use of existing discrete cosine transform (DCT) software and hardware modules for fast processing and easy implementation. 1.6 The Applicant thus submits that D2-D4 do not disclose application of a reversible 2D overlap operator to a first array of digital media data that is offset in both the horizontal and vertical directions from borders of the macro blocks, where the application comprises applying a series of operations comprising horizontal operations of a 1D reversible overlap operator interleaved with vertical operations of the 1D reversible overlap operator. Further, D2-D4 do not disclose application of a reversible 2-D block transform to a second array of digital media data that is aligned with the borders of the macro blocks. 1.7 The above-mentioned differentiating features provides a technical advancement separating the one-dimensional overlap operator into stages, and interspersing the stages of the horizontal and vertical application of the overlap operator. This, in turn, allows implementation of a normalized scaling operation to more limited subsets of the data block by noting cancellation of "cross terms" in the interspersed 2D structure. An efficient scale-free reversible 2D pre/post filter is thus obtained. 1.8 Therefore, the Applicant submits that the subject matter claimed in the amended independent claim 1 include following one or more inventive features: "… applying a reversible 2-dimensional overlap operator to a first array of digital media data (1520) that is offset in both the horizontal and vertical directions from borders of the macro blocks; and applying a reversible 2-dimensional block transform to a second array of digital media data (1510) that is aligned with the borders of the macro blocks, the second array of digital media (1510) data including data resulting from the application of the reversible 2-dimensional overlap operator, wherein the applying the reversible 2-dimensional overlap operator and the reversible 2-dimensional block transform together effect the lapped transform of the 2-dimensional digital media data (410) and wherein, the applying the reversible 2-dimensional overlap operator comprises, for the first array of digital media data, applying a series of operations (2100) comprising horizontal operations of a 1- dimensional reversible overlap operator interleaved with vertical operations of the 1-dimensional reversible overlap operator" 1.9 The Applicant thus asserts that it would not be obvious to a person skilled in the art to combine the teachings of D2, D3, and D4, in combination with common general knowledge, to arrive at the subject matter claimed in the amended independent claim 1. Therefore, the subject matter as claimed in amended independent claim 1 involves an inventive step over D2-D4. 1.10 As pending independent claim 11 recites similar features as that of amended independent claim 1, independent claim 11 also involves an inventive step over D2- D4. 1.11 Further, the amended dependent claims 2-10 and 12-15 also involve an inventive step due to their dependence on amended independent claims 1 and 11. The objection related to inventive step is thus addressed.

After going through the above submissions of the applicant agent , it is found that the following are the distinguishing features of the present invention which makes it novel and inventive over cited prior art D1-D4:

> applying a reversible 2-dimensional overlap operator to a first array of digital media data (1520) that is offset in both the horizontal and vertical directions from borders of the macro blocks; and applying a reversible 2-dimensional block transform to a second array of digital media data (1510) that is aligned with the borders of the macro blocks, the second array of digital media (1510) data including data resulting from the application of the reversible 2-

dimensional overlap operator, wherein the applying the reversible 2-dimensional overlap operator and the reversible 2-dimensional block transform together effect the lapped transform of the 2-dimensional digital media data (410) and wherein, the applying the reversible 2-dimensional overlap operator comprises, for the first array of digital media data, applying a series of operations (2100) comprising horizontal operations of a 1- dimensional reversible overlap operator interleaved with vertical operations of the 1-dimensional reversible overlap operator"

In view of the above findings, objection under section 2(1) (j) has been met.

Regarding objection 2 of hearing notice: Section 3(k):

The independent claim 1 and 11 as amended are given below for ready reference:

Claim-1:

1. A method of encoding 2-dimensional digital media data (410) , the method comprising: inputting the 2-dimensional digital media data (410) using an input device (4750); and compressing by a processing unit (4710), the 2-dimensional digital media (410) into a compressed bitstream (420) using a lapped transform, wherein the compressing comprises: partitioning the 2-dimensional digital media data (410) into macro blocks; applying a reversible 2-dimensional overlap operator to a first array of digital media data (1520) that is offset in both the horizontal and vertical directions from borders of the macro blocks; and applying a reversible 2-dimensional block transform to a second array of digital media data (1510) that is aligned with the borders of the macro blocks, the second array of digital media (1510) data including data resulting from the application of the reversible 2-dimensional overlap operator, wherein the applying the reversible 2-dimensional overlap operator and the reversible 2-dimensional block transform together effect the lapped transform of the 2-dimensional digital media data (410) and wherein, the applying the reversible 2-dimensional overlap operator comprises, for the first array of digital media data, applying a series of operations (2100) comprising horizontal operations of a 1- dimensional reversible overlap operator interleaved with vertical operations of the 1 dimensional reversible overlap operator.

Claim-11:

A 2-dimensional digital media processor, comprising: a data storage buffer (4740) for storing 2-dimensional digital media data (410) to be processed using a lapped transform; a processor (4710) programmed to: compress the 2-dimensional digital media (410) into a compressed bitstream (420) by a processing unit (4710) using a lapped transform, wherein the compressing comprises: partitioning the 2-dimensional digital media data (410) into macro blocks; applying a reversible 2-dimensional overlap operator to a first array of digital media data (1520) that is offset in both the horizontal and vertical directions from borders of the macro blocks; and applying a reversible 2-dimensional block transform to a second array of digital media data (1510) that is aligned with the borders of the macro blocks, the second

array of digital media data (1510) including data resulting from the application of the reversible 2-dimensional overlap operator, wherein the applying the reversible 2-dimensional overlap operator and the reversible 2-dimensional block transform together effect the lapped transform of the 2-dimensional digital media data (410) and wherein, the applying the reversible 2- dimensional overlap operator comprises, for the first array of digital media data, applying a series of operations (2100) comprising horizontal operations of a 1-dimensional reversible overlap operator interleaved with vertical operations of the 1 dimensional reversible overlap operator.

Section 3(k):

Submission of the applicant has been considered. However, the alleged invention falls within the scope of section 3(k) of the Patents Act as: The applicant in written submission to hearing dated 15.03.2019 quoted two court cases

1) Delhi High Court's decision in the case of TELEFONAKTIEBOLAGET LM ERICSSON v. INTEX TECHNOLOGIES (INDIA) LIMITED [CS(OS) No.1045/ 2014].
2) HTC Europe Co. Ltd v. Apple Inc. [2013] EWCA Civ 451, decided by the UK Court of Appeals.

The above court cases cannot be held applicable to the present invention. Particularly from the specification page 32 wherein it is clear that the invention is mainly performed by the software The processing unit (4710) executes computer-executable instructions and may be a real or a virtual processor. In a multi-processing system, multiple processing units execute computer-executable instructions to increase processing power. The memory (4720) may be volatile memory (e.g., registers, cache, RAM), non-volatile memory (e.g., ROM, EEPROM, flash memory, etc.), or some combination of the two. The memory (4720) stores software (4780) implementing the described encoder/decoder and transforms. A computing environment may have additional features. For example, the computing environment (4700) includes storage (4740), one or more input devices (4750), one or more output devices (4760), and one or more communication connection.

Further the present invention refers operating system, software provides an operating environment for other software executing in the computing environment (4700), and coordinates activities of the components of the computing environment (4700). The storage (4740) may be removable or non-removable, and includes magnetic disks, magnetic tapes or cassettes, CD-ROMs, CD-RWs, DVDs, or any other medium which can be used to store information and which can be accessed within the computing ' environment (4700). The storage (4740) stores instructions for the software (4780) implementing the codec based on a lapped transform using the 4x4 pre/post-filtering.

Guidelines for Examination of Computer-related Inventions (CRIs) published on 19.02.2016 and issued vide office order no. CG/office order/2016/179 dated 19.02.2016, in chapter 5 on page 18 states: "If the contribution lies in the field of computer programme, check whether it is claimed in conjunction with a novel hardware and proceed to other steps to determine patentability with respect to the invention. The computer programme in itself is never patentable. If the contribution lies solely in the computer programme, deny the claim. If the contribution lies in both the computer programme as well as hardware, proceed to other steps of patentability." Hence, amended claims 1-15 fall u/s 3(k) as claims recite method wherein a specially programmed Processor generates intermediates value to achieve a 2-dimensional digital media data . While electronic hardware is recited it may merely be a general purpose hardware on which the method operates.

In view of contribution lying solely in the computer programme, claims 1-15 are not allowable under section 3(k) of the Patents Act, 1970 (as amended).

Conclusion:

The argument submitted by the agent has been carefully considered, but the requirement of Para 2 of the hearing notice is not met. The amended claims 1-15 are not allowed u/s 3(k) as the claimed invention fall under computer program.

After careful consideration of the facts and submission made by the agent of the applicant during hearing as well as all the documents on record, the application does not meet the objections communicated in the hearing notice. Hence the instant application is hereby refused for grant of patent on amended set of claims 1-15 filed on 15/03/2019 under section 3(k) of the Patents Act.

(Santosh K.Mehtry)

Asstt.Controller of Patent & Designs)

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